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Phase locked 270–440 GHz local oscillator based on flux flow in long Josephson tunnel junctions

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The combination of narrow linewidth and wide band tunability makes the Josephson flux flow oscillator (FFO) a perfect on-chip local oscillator for integrated sub-mm wave receivers for, e.g., spectral radio astronomy. The feasibility of phase locking the FFO to an external reference oscillator is demonstrated experimentally. A FFO linewidth as low as 1 Hz (determined by the resolution bandwidth of the spectrum analyzer) has been measured in the frequency range 270–440 GHz relative to a reference oscillator. This linewidth is far below the fundamental level given by shot and thermal noise of the free-running tunnel junction. The results of residual FFO phase noise measurements are also presented. Finally, we propose a single-chip fully superconductive receiver with two superconductor–insulator–superconductor mixers and an integrated phase-locked loop.
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I. INTRODUCTION

The Josephson flux flow oscillator (FFO)[1] has proven to be a reliable wide band and easy tunable local oscillator suitable for integration with a superconductor–insulator–superconductor (SIS) mixer in a single-chip sub-millimeter wave receiver.[2] A DSB noise temperature below 100 K has been achieved for an integrated receiver with the FFO operating near 500 GHz.[3] The antenna beam, approximately $f/10$ with sidelobes below -17 dB,[3] makes the integrated receiver suitable for coupling to the real telescope. For spectral radio-astronomy applications besides the noise temperature and the antenna beam pattern, the frequency resolution of the receiver, which is determined by both the instant linewidth of the local oscillator and its long-time stability, should be much less than 1 ppm of the center frequency. Recently a reliable technique for linewidth measurements was developed[4] and a free-running FFO linewidth as low as a few hundred kHz has been observed.[4,5] The reduction of the linewidth obtained by phase locking described below significantly improves the spectral resolution of the sub-mm receiver. Equally important is that the coexisting wide band lock-in tunability of the FFO enables a large spectral coverage.

II. LINEWIDTH AND TUNING OF THE FFO

The FFO is a *long* Josephson tunnel junction in which an applied dc magnetic field and a bias current drive a unidirectional flow of fluxons, each containing one magnetic flux quantum $\Phi_0 = h/2e \approx 2\times10^{-15}$ Wb. Symbol h is Planck's constant and e is the electron charge. The junction is one-dimensional with length $L \gg \lambda_J$ and width $W \ll \lambda_J$, where λ_J is the Josephson penetration length. An integrated control line with current I_{CL} is used to generate the dc magnetic field applied to the FFO. The velocity and density of the fluxons and thus the power and frequency of the emitted mm wave signal may be easily tuned by either of the two external parameters. According to the Josephson relation the junction biased at voltage V oscillates with a frequency $f = (1/\Phi_0)\,V$, where the prefactor equals 483.6 GHz/mV. The damping of the FFO is characterized by the shunt damping parameter $\alpha = 1/\sqrt{\beta_c}$, where β_c is the McCumber parameter.

Presently no reliable theory exists for the FFO linewidth and preliminary estimations[6] have to be made on the basis of the general theory for the radiation linewidth of the *lumped* Josephson tunnel junction.[7] The linewidth, Δf, of a Josephson junction is mainly determined by low frequency current fluctuations. For white noise it can be written (see, e.g. Ref. 8) as

$$\Delta f = (2\pi/\Phi_0^2)(R_d^B)^2 S_i(0), \tag{1}$$

where $S_i(0)$ is the density of the low frequency current fluctuations, and $R_d^B = \partial V/\partial I_B$ is the dc differential resistance which transforms the current fluctuations to voltage (and phase) noise. For a lumped tunnel junction[7,8]

$$S_i(0) = (e/2\pi) I_B(V_{\mathrm{dc}}) \coth(v), \quad \text{with} \quad v = (eV_{\mathrm{dc}})/(2k_B T_{\mathrm{eff}}), \tag{2}$$

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where k_B is Boltzmann's constant. I_B and V_{dc} are the current and averaged dc voltage in the bias point. T_{eff} is the effective temperature of the quasiparticles in the junction electrodes. This formula describes a nonlinear superposition of thermal and shot noise. It should be noted that the formula does not take into account the spatial variation of the tunnel current along the FFO, the interactions of the moving fluxons, and the influence of the external low frequency interference. All these effects are believed to increase the FFO linewidth.

Fluctuations in the external magnetic field can be accounted for by the differential tuning resistance of the control line $R_d^{CL} = \partial V_{FFO} / \partial I_{CL}$ for fixed dc bias current I_B. In the case of an *external interference* both the ''usual'' differential resistance R_d^B and R_d^{CL} ''convert'' low frequency external noise currents, $I_{lf}^{(B,CL)}$, to frequency fluctuations following the same relations:

$$\Delta f \propto R_d^{(B,CL)} * I_{lf}^{(B,CL)}. \tag{3}$$

According to Eqs. (1) and (3) the radiation linewidth may be reduced by lowering the spectral noise density and/or the differential resistance at low frequencies, $f < \Delta f$. This can be done by appropriate shunting of the junction at low frequencies and/or suppression of the current fluctuations by an external phase-locked loop (PLL) system with a bandwidth larger than Δf with feedback through either of the two bias current channels. In this article a significant reduction of the FFO linewidth relative to that of the intrinsic FFO linewidth (determined by wide band thermal fluctuations) is demonstrated experimentally by using an external electronic PLL.

III. EXPERIMENTAL SETUP

A block diagram of the setup for linewidth measurements is shown in Fig. 1. Details of the chip design are published elsewhere.[4,5] The FFO linewidth is measured in the frequency range up to 600 GHz with a new experimental technique.[4] The sub-mm wave signal coming from the FFO is mixed in the SIS Josephson mixer with the nth harmonic of the external synthesizer frequency f_{SYN} (about 10 GHz). In order to prevent the external oscillator signal (as well as its low harmonics) from reaching the FFO a high-pass microstrip filter with a cut-off frequency of about 200 GHz is used. The intermediate frequency (IF) signal with frequency, $f_{IF} = \pm(f_{FFO} - n f_{SYN})$ is amplified in a cooled amplifier with noise temperature $T_n \approx 20$ K and 27 dB gain. After additional room temperature amplification the signal enters the PLL system. A small fraction of the signal is applied via the directional coupler to a spectrum analyzer which is also phase locked to the synthesizer by a common 10 MHz reference signal. By using this technique the downconverted FFO spectrum is measured (see Fig. 2). The spectrum recorded is the difference between the FFO signal and the nth harmonic of the synthesizer, and thus the FFO phase noise is measured relative to the appropriate synthesizer harmonic.

In the PLL unit the signal frequency is divided by four and in a frequency-phase discriminator compared with a 100 MHz reference signal also phase locked to the main 10 GHz synthesizer. The output signal proportional to the phase difference is returned via the loop bandwidth regulator (maximum bandwidth about 10 MHz) to the FFO current bias through the coaxial cable and the cold 50 Ω resistor mounted on the bias plate. The same coaxial cable that enters the cryostat is used for both the 10 GHz synthesizer signal and the PLL control output. The couplers with microstrip filters are used to combine and split these signals.

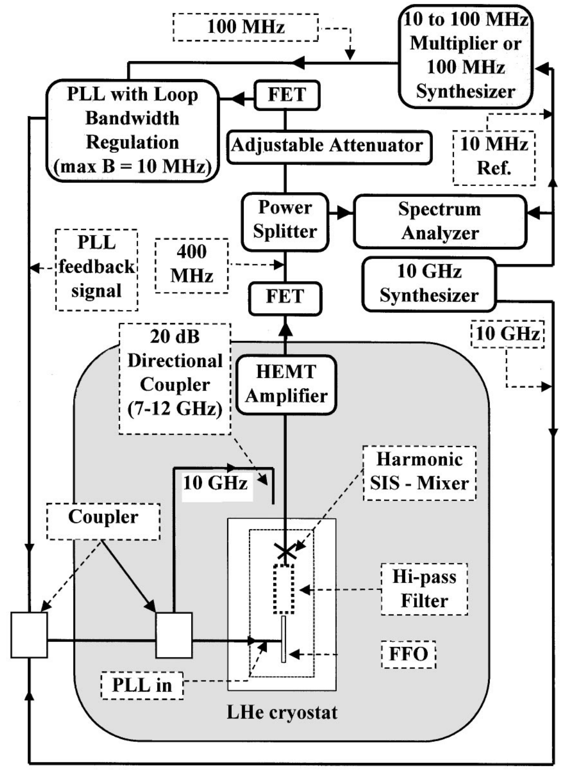

FIG. 1. Block diagram of the PLL circuit and linewidth measurement setup. The central components are the cryogenic chip with its FFO and SIS mixer, the cooled low-noise 400 MHz high electron mobility transistor IF amplifier, and the 10 GHz synthesizer, that also generates the 10 MHz reference signals for the spectrum analyzer and the phase detector in the PLL.

In order to perform accurate linewidth measurement the IF spectra have to be averaged with a sufficiently small video bandwidth. The PLL system with a relatively low loop gain and narrow bandwidth setting (< 10 kHz) can be used for *frequency locking* of the FFO to the 10 GHz synthesizer in order to measure the linewidth, Δf_{AUT}, of the free-running FFO. In this case the spectral shape of the measured linewidth is rather wide but the average frequency remains stable.

IV. RESULTS AND DISCUSSION

It was experimentally found[6] that the PLL system can considerably narrow the FFO linewidth if Δf_{AUT} (measured at the −3 dB level) is smaller than the PLL regulation bandwidth, B_{PLL}. Opposite to the case described above where $\Delta f_{AUT} > B_{PLL}$ only frequency locking without a noticeable linewidth change is achieved. In the intermediate range where Δf_{AUT} is comparable to but smaller than $B_{PLL} (2.5\,\mathrm{MHz} < \Delta f_{AUT} < 10\,\mathrm{MHz})$ there is an increase of the FFO power at the central frequency while the FFO linewidth is reduced (measurements were done at FFO bias points with

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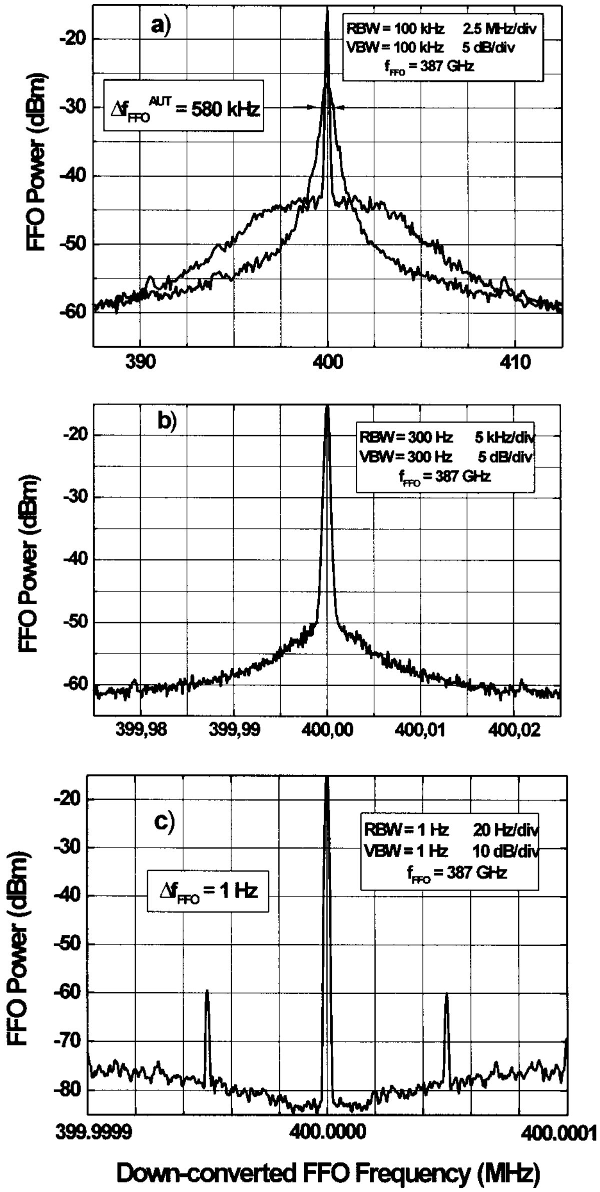

FIG. 2. The down converted IF power spectra of the FFO ($f = 387$ GHz) recorded with different frequency spans clearly demonstrate the phase locking.

different values of R_d^B and R_d^{CL}). Full phase locking takes place for $\Delta f_{AUT} < 2.5$ MHz. Figure 2 shows typical IF power spectra of the phase-locked FFO measured at $f_{\mathrm{FFO}} = 387$ GHz for different settings of the spectrum analyzer. A FFO linewidth as low as 1 Hz is presented in Fig. 2(c). This value is actually determined by the limited resolution bandwidth of the spectrum analyzer. It means that the FFO linewidth can be reduced below the value determined by the fundamental shot and thermal fluctuations of the free-running tunnel junction.

A consequence of the phase locking is the appearance of a vertical step ($R_d^B = 0$) in the dc current-voltage characteristic (IVC) of the FFO at the voltage corresponding to the frequency f_{FFO} where the FFO is locked; see Eq. (1). The position of this step is also insensitive to small changes in the control line current, and accordingly also $R_d^{\mathrm{CL}} = 0$. A hold-in range of the FFO bias voltage as large as 1.5 μV has been experimentally measured. This corresponds to an effective PLL regulation band of about 750 MHz. The pull-in limit depends on the position of the operation point on the resonant Fiske step (FS), and it was approximately equal to the hold-in range. It should be noted that this step is not a harmonic Shapiro step. First, it is shifted from the appropriate position by 0.8 μV (corresponding to the PLL input frequency 400 MHz). Furthermore, the position of the vertical step can be tuned precisely by changing the reference signal. A reference signal in the frequency range of 90–110 MHz can be applied from a second synthesizer phased locked to the first one (see Fig. 1) in steps of 0.1 Hz (minimum increment of the synthesizer). This corresponds to a voltage accuracy of 2×10^{-16} V.

It should be noted that phase locking of the FFO presently has only been realized on steep FSs, where the free-running FFO linewidth is about 1 MHz due to the small values of R_d^B. Experimentally an increase of the FFO linewidth has been found at voltages higher than a certain boundary voltage, V_b;[5] correspondingly, the IVC of the FFO is modified and the internal damping increases abruptly at this threshold. The boundary voltage $V_b \approx 950\,\mu$V (for Nb–AlO$_x$–Nb tunnel junctions) $\approx$ 1/3 of the superconductor gap voltage, V_g. A simple model based on Josephson radiation self-coupling (JSC)[9] was introduced[5] to explain the experimentally measured IVC. The JSC caused by the absorption of the internal ac Josephson radiation photons by the quasiparticles results in current ''bumps'' at the voltage $V_{\mathrm{JSC}} = V_g/(2n+1)$, which gives $V_{\mathrm{JSC}} = V_g/3$ for $n = 1$. The effect of self-pumping explains the abrupt vanishing of the FS for $V > V_g/3$ due to the strongly increased damping.[10]

For operation at all FFO voltages including $V > V_b$ additional efforts should be undertaken to decrease the dynamic resistance and thus the initial FFO linewidth. Also an ultrawide band PLL system with sufficiently low phase noise is needed. In this context the ongoing development of an on-chip integrated phase detector looks very promising. The PLL bandwidth in this case will not be limited by the electrical properties of the long interconnection cables. Also, a number of stability and noise problems related to electronics kept at room temperature may be avoided. The cryogenic phase detector, low noise amplifiers, etc. can be constructed using existing superconducting electronic components.

The residual phase noise of the phase-locked FFO (measured relative to the reference synthesizer) is plotted in Fig. 3 (data from Fig. 2) as function of the offset from the 400 MHz carrier. The specification and measured data for the synthesizer used (HP83752B) are shown in Fig. 3 as well. Actually the FFO was locked to the 36th harmonic of the synthesizer at this measurement, and to get the real FFO phase noise one should add to the measured residual FFO phase noise the synthesizer noise multiplied by $n^2 = 1296$ as shown in Fig. 3. The advantage of this scheme is that the spectral purity of the fixed frequency low frequency reference oscillator is transferred to the FFO which operates at a much higher frequency. Even more important is that the phase-locked FFO, while being tuned over a wide frequency band, maintains this low phase noise. The problem no longer is to reduce the intrinsic linewidth of the free-running FFO but merely to get

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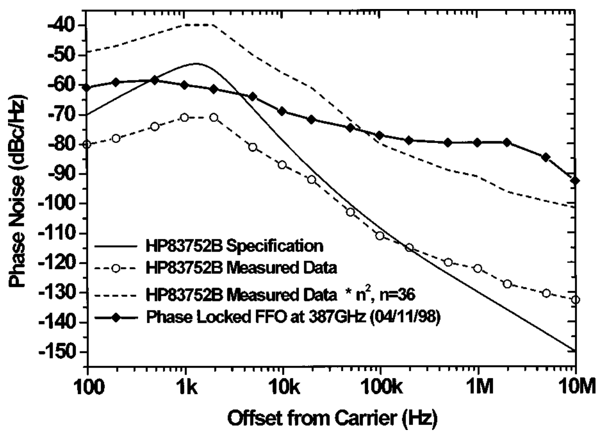

FIG. 3. Experimentally measured phase noise of the phase-locked FFO at 387 GHz compared with the data for the 10 GHz HP83752B synthesizer. Since the residual phase noise of the FFO is measured relative to the 36th harmonic of the synthesizer, one must add its phase noise multiplied by $36^2=1296$ in order to get the total phase noise of the phase-locked FFO.

the low phase noise reference oscillator and the wide band PLL.

The results given above demonstrate our ability to control and significantly narrow the linewidth of a Josephson oscillator using an external electronic PLL system, provided that the PLL bandwidth is larger than the intrinsic linewidth of the Josephson oscillator. Even at the present state of development the integrated receiver with the PLL system is applicable for practical spectral radio astronomy in the frequency range of 400–450 GHz.

In this frequency range the Fiske steps of our Nb–AlO_x–Nb FFO are closely spaced and almost overlap because of the dispersion of the long Josephson tunnel junction.[10] The frequency gaps between the bands on subsequent FSs where FFO phase locking is possible are considerably smaller than 8 GHz. It means that frequencies within these gaps can be covered by the FFO when it is biased on a neighboring FS by using a wide band IF amplifier with a bandwidth of up to 4 GHz, resulting in an integrated receiver with continuous frequency coverage and complete phase locking.

A low value of the damping coefficient, α, in the long junction gives steep FSs with small R_d^B (high-Q Fiske resonances) while the voltage difference between successive FSs scales inversely with the junction length L. So with the present limitations of the PLL bandwidth optimization of the FFO parameters, e.g., those based on numerical simulations, is needed in order to extend the frequency range of phase-locked operation to frequencies above approx 500 GHz ($V \geqslant V_b$) where Josephson self-coupling and surface resistance in the superconducting films increase the damping considerably. It is still an experimental challenge to obtain phase-locked operation of the FFO in the ''true'' flux flow regime where the normalized damping $\alpha L/\lambda_f \geqslant \pi$ (approaching the Eck limit[10]).

V. FUTURE DEVELOPMENTS OF THE INTEGRATED RECEIVER

An all-superconducting phase-locked integrated receiver has been proposed based on the above technique for phase locking of the FFO.[6] In this concept two separate SIS mixers are placed on one chip and both connected at high frequencies to the same FFO. One SIS mixer serves as the heterodyne detector in the receiver while the other is used for phase locking the FFO to a reference oscillator. Using this concept a prototype 350 GHz integrated superconducting heterodyne receiver containing a phase-locked flux-flow oscillator has been designed and fabricated. The circuit (see Fig. 4) of the single-chip receiver contains one FFO as a common local oscillator for both a high-quality quasioptical low-noise SIS mixer/detector and a harmonic SIS mixer (eventually with a SIS frequency multiplier, optional) for the PLL circuit. The FFO is phase locked to the 35th harmonic of an external 10 GHz synthesized low-phase noise source using custom-designed room temperature electronics with a PLL loop bandwidth B_{PLL} of about 10 MHz and IF frequency $f_{\mathrm{IF}} = 400\,\mathrm{MHz}$. Testing of the novel chip is in progress. In the future one also may integrate on the receiver chip the reference oscillator, the PLL circuitry, the IF amplifiers, and an analog/digital converter for fast pre-processing of data. All components may be fabricated with the present superconductor technology.

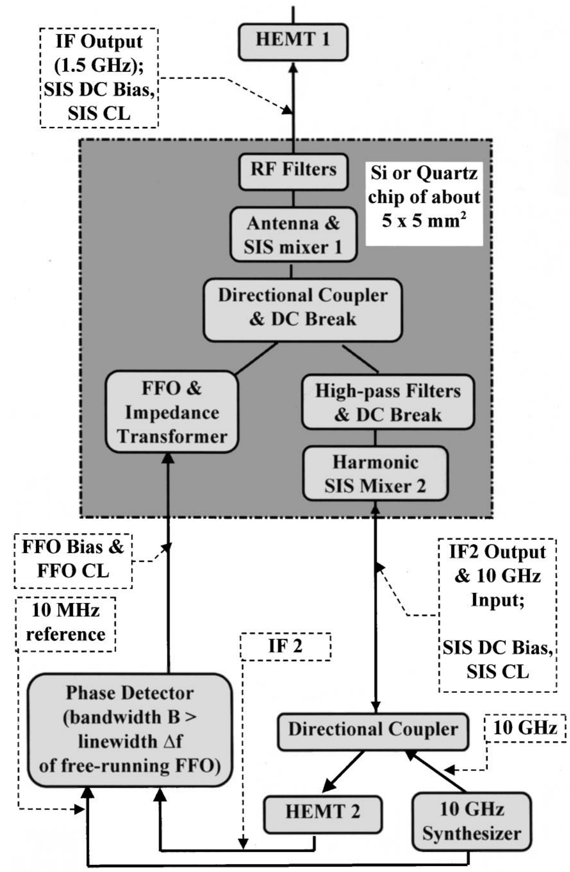

FIG. 4. Block diagram of the proposed submillimeter all-superconducting phase-locked single-chip integrated receiver. The common FFO supplies two SIS mixers, one serves as the detector/mixer, and the other facilitates the phase locking and tuning (see the text) of the FFO via the PLL circuit.

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